

Circuit Description

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Notes:

- For a good understanding of the following circuit descriptions, please use the [Block diagram](#). Where necessary, you will find a separate drawing for clarification.
- Figures below can deviate slightly from the actual situation, due to different set executions.

Introduction

The 'L01.1U AC' chassis is a global TV chassis for the model year 2003 and is used for TV sets with screen sizes from 20" - 32" (large screen), in Super Flat, Real Flat, and Wide Screen executions. In comparison to its predecessor (the 'L01.1U AB'), the chassis has enhanced features like a 2D 3-line Comb-filter and 'Active Control'.

The standard architecture consists of a Main panel, a Picture Tube panel, a Side I/O panel, and a Top Control panel.

The Main panel consists primarily of conventional components with hardly any surface mounted devices.



Figure: Mono Carrier component side

The functions for video processing, microprocessor (P), and teletext (TXT) decoder are combined in one IC (TDA958xH), the so-called Ultimate One Chip (UOC). This chip is (surface) mounted on the copper side of the LSP.

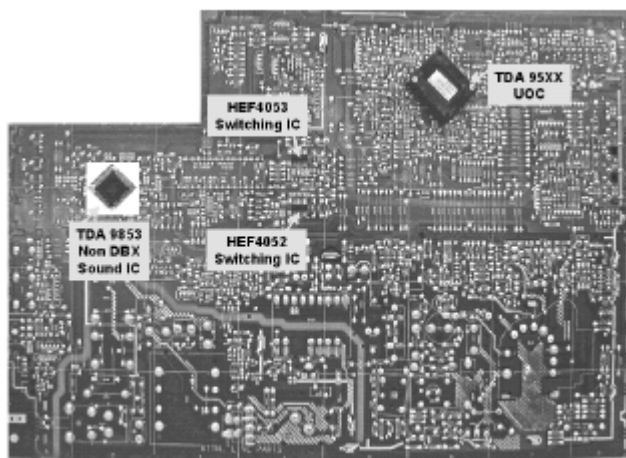


Figure: Mono Carrier solder side

The 'L01.1U AC' is divided into 2 basic systems, i.e. mono and stereo sound. While the audio processing for the mono sound is done in the audio block of the UOC, an external audio processing IC is used for stereo sets.

The tuning system features 181 channels with on-screen display. The main tuning system uses a tuner, a microcomputer, and a memory IC mounted on the main panel.

The microcomputer communicates with the memory IC, the customer keyboard, remote receiver, tuner, signal processor IC and the audio output IC via the I2C bus. The memory

IC retains the settings for favorite stations, customer-preferred settings, and service / factory data.

The on-screen graphics and closed caption decoding are done within the microprocessor, and then sent to the signal processor IC to be added to the main signal.

The chassis utilizes a Switching Mode Power Supply (SMPS) for the main voltage source. The chassis has a 'hot' ground reference on the primary side and a cold ground reference on the secondary side of the power supply and the rest of the chassis.

Audio Signal Processing

Stereo

In stereo sets, the signal goes via the SAW filter (position 1002/1003), to the audio demodulator part of the UOC IC 7200. The audio output on pin 33 goes to the stereo decoder 7831/ 7861. The switch inside this IC selects either the internal decoder or an external source.

There are two stereo decoders versions used:

1. A BTSC DBX stereo/SAP decoder (MSP34X5 at position 7831) for the highest specified sets, and
2. A BTSC non-DBX stereo decoder (TDA9853 at position 7861) for BTSC Economic.

The output is fed to the to the audio amplifier (AN7522 at position 7901). The volume level is controlled at this IC (pin 9) by a control line (Volume|Mute) from the microprocessor. The audio signal from 7901 is then send to the speaker and headphone output panel.

[Stereo audio signal processing](#)

Mono

In mono sets, the signal goes via the SAW filter (position 1002/1003), to the audio demodulator part of the UOC IC 7200. The audio output on pin 48 goes to the audio amplifier (AN7523 at position 7902).

The volume level is controlled at this IC (pin 9) by a 'VolumeMute' control line from the microprocessor.

The audio signal from IC 7902 is then send to the speaker and headphone output panel.

[Mono audio signal processing](#)

Video Signal Processing

Introduction

The video signal-processing path consists of the following parts:

- RF signal processing.
- Video source selection.
- Video demodulation.
- Luminance / Chrominance signal processing.
- RGB control.
- RGB amplifier

The processing circuits listed above are all integrated in the UOC TV processor. The surrounding components are for the adaptation of the selected application. The I2C bus is for defining and controlling the signals.

RF Signal Processing

The incoming RF signal goes to the tuner (pos. 1000), where the 45.75 MHz IF signal is developed and amplified. The IF signals then exits the tuner from pin 11 to pass through the SAW filter (pos. 1002/1003). The shaped signal is then applied to the IF processor part of the UOC (pos. 7200).

Tuner AGC (Automatic Gain Control) will reduce the tuner gain and thus the tuner output voltage when receiving strong RF signals. Adjust the AGC takeover point via the Service Alignment Mode (SAM). The tuner AGC starts working when the video-IF input reaches a certain input level and will adjust this level via the I2C bus. The tuner AGC signal goes to the tuner (pin 1) via the open collector output (pin 22) of the UOC.

The IC also generates an Automatic Frequency Control (AFC) signal that goes to the tuning system via the I2C bus, to provide frequency correction when needed.

The demodulated composite video signal is available at pin 38 and then buffered by transistor 7201.

Video Source Selection

The Composite Video Blanking Signal (CVBS) from buffer 7201 goes to the audio carrier trap filters 1200, 1201, or 1202 (depending on the system used), to remove the audio signal. The signal then goes to pin 40 of IC 7200. The internal input switch selects the following input signals:

- Pin 40: terrestrial CVBS input
- Pin 42: external AV1 CVBS input
- Pin 44: external Side I/O CVBS or AV2 (or comb filter) luminance (Y) input
- Pin 45: external AV2 (or comb filter) chrominance (C) input

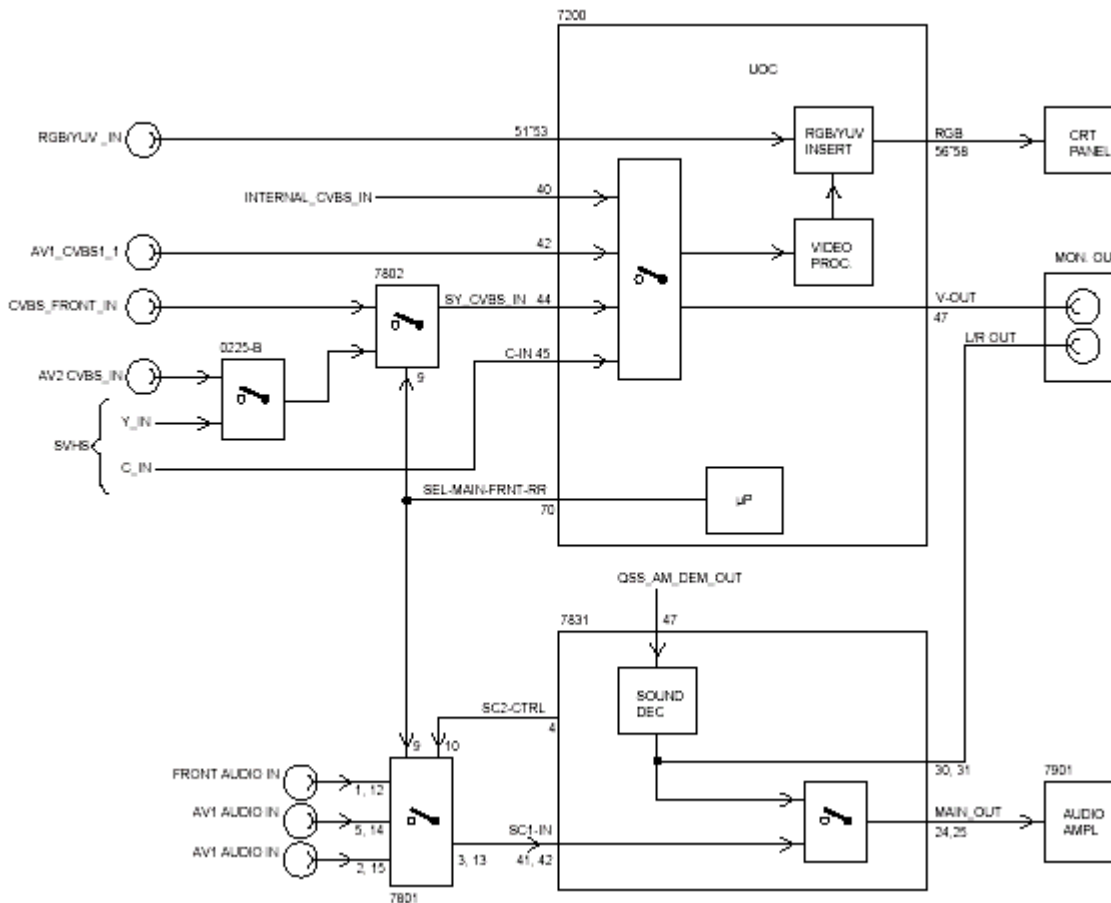


Figure: Video source selection

Once the signal source is selected, a chroma filter calibration is performed. The received color burst sub-carrier frequency is used for this. Correspondingly, the chroma band pass filter for PAL/NTSC processing or the cloche filter for SECAM processing is switched on. The selected luminance (Y) signal is supplied to the horizontal and vertical synchronization circuit and to the luminance processing circuit. In the luminance-processing block, the luminance signal goes to the chroma trap filter. This trap is switched 'on' or 'off' depending on the color burst detection of the chroma calibration circuit. The group delay correction part can be switched between the BG and a flat group delay characteristic. This has the advantage that in multi-standard receivers no compromise has to be made for the choice of the SAW filter.

Comb Filter

Introduction

The video signal prepared for broadcast contains two major parts commingled, the luminance (makes a black and white picture in full detail) and chrominance (coloration with not quite all the detail). This method is used instead of red, green, and blue sub-signals in

order to get the best looking picture that can be transmitted in the limited bandwidth of the broadcast channel.

Every TV receiver and VCR must contain a filter to separate the luminance and color (Y and C) again. Less than perfect Y/C separators lose resolution -- horizontal, vertical, or both. Also there are artifacts such as *rainbow swirls* where thin stripes should be, and *crawling dots* where patches of different colors meet. The perfect Y/C separator does not exist yet, although some 3D comb filters come close.

There are several methods for filtering:

- **No comb filter.** The cheapest solution is to use simple filters (notch, low pass, bandpass filters) that pass only the coarse and medium horizontal detail (lower 3 MHz or so) to the luminance circuits and pass the bulk of the color information still commingled with the fine luminance detail (3 to 4.2 MHz) to the color circuits.
- **Two line ordinary filter.** The improvements over 'no' comb filter are: revealing of finer horizontal detail overall, and some reduction of rainbow swirls. Improvement of fine detail is most prominent where details consist of upright dark and light lines.
- **Three line ordinary filter.** Improvement over the two line filter consists of sharper transition from one color to another at sharp horizontal color boundaries, and less dot crawl.
- **Three line adaptive (a.k.a. 2D; dynamic) filter.** This method adapts the mixing according the line content of two fields. The big improvement that the 2D comb filter brings, is the elimination (or near elimination) of dot crawl. This type of filter is used in the 'L01.1U AC' chassis. When present, the filter CBA is plugged-in on connector 1810B of the Main panel.
- **Motion adaptive (3D) filter.** The difference with the 2D method is that this method uses three fields, so it also uses 'time' dimension. The 3D comb filter can achieve essentially perfect Y/C separation, eliminating all dot crawl and rainbow swirls for 'stationary' subject material, and perform at least as well as the 2D filter for the rest of the picture.

Implementation

The input (CVBS) signal comes from pin 47 of the the UOC. On the comb filter panel, it first enters a low-pass filter (items 2409, 5408, 2408, 5407, and 2407) and an amplifier circuit (items 7401 and 7402). The LPF is used to eliminate the noise and the amplifier circuit to get a video input of $1 V_{PP}$.

The 'REF0' subcarrier reference (f_{SC}) is fed to pin 11 and internally multiplied by four ($4 \times 3.58 \text{ MHz} = 14.32 \text{ MHz}$) for the system clock.

After processing, the Y/C outputs (pins 25 and 23) are both filtered by a low-pass filter, in order to eliminate the high frequency harmonics of this system clock.

After filtering, the Y and C signals are fed to the source inputs of the UOC (pins 44 and 45).

Specification

If the comb filter is 'on', and the signal level drops below a specified value, then the filter is set to 'off'. Once the filter is set to 'off' it will remain 'off' until a channel change is performed.

When an S-Video (Y/C) or component video signal is offered to the TV, the filter is bypassed via the 'COMB_BYPASS' signal from the microprocessor.

Video Demodulation

The color decoder circuit detects whether the signal is a PAL, NTSC, or SECAM signal. The result is made known to the auto system manager. The PAL/NTSC decoder has an internal clock generator, which is stabilized to the required frequency by using the 12 MHz clock signal from the reference oscillator of the microcontroller / teletext decoder.

The base-band delay line is used to obtain a good suppression of cross color effects. The Y signal and the delay line outputs U and V are applied to the luminance / chroma signal processing part of the TV processor.

Luminance / Chrominance signal Processing

The output of the YUV separator is fed to the internal YUV switch, which switches between the output of the YUV separator or the external YUV (for DVD or PIP) on pins 51-53. Pin 50 is the input for the insertion control signal called 'FBL-1'. When this signal level becomes higher than 0.9 V (but less than 3 V), the RGB signals at pins 51, 52, and 53 are inserted into the picture by using the internal switches.

Also, some picture improvement features are implemented in this part:

- **Black stretch.** This function corrects the black level of incoming signals, which have a difference between the black level and the blanking level. The amount of extension depends upon the difference between actual black level and the darkest part of the incoming video signal level. It is detected by means of an internal capacitor.
- **White stretch.** This function adapts the transfer characteristic of the luminance amplifier in a non-linear way depending on the average picture content of the luminance signal. It operates in such a way that maximum stretching is obtained when signals with a low video level are received. For bright pictures, stretching is not active.
- **Dynamic skin tone correction.** This circuit corrects (instantaneously and locally) the hue of those colors, which are located in the area in the UV plane that matches the skin tone. The correction is dependent on the luminance, saturation, and distance to the preferred axis.

The YUV signal is then fed to the color matrix circuit, which converts it to R, G, and B signals.

The OSD/TXT signal from the microprocessor is mixed with the main signal at this point, before being output to the CRT board (pins 56, 57, and 58).

RGB Control

The RGB control circuit enables the picture parameters contrast, brightness, and saturation to be adjusted, by using a combination of the user menus and the remote control.

Additionally automatic gain control for the RGB signals via cut-off stabilization is achieved in this functional block to obtain an accurate biasing of the picture tube. Therefore, this block inserts the cut-off point measuring pulses into the RGB signals during the vertical retrace period.

The following additional controls are used:

- **Black current calibration loop.** Because of the 2-point black current stabilization circuit, both the black level and the amplitude of the RGB output signals depend on the drive characteristics of the picture tube. The system checks whether the returning measuring currents meet the requirements, and adapt the output level and gain of the circuit when necessary. After stabilization of the loop, the RGB drive signals are switched on. The 2-point black level system adapts the drive voltage for each cathode in such a way that the two measuring currents have the right value. This is done with the measurement pulses during the frame flyback. During the first frame, three pulses with a current of 8 μA are generated to adjust the cut off voltage. During the second frame, three pulses with a current of 20 μA are generated to adjust the 'white drive'. This has as a consequence, that a change in the gain of the output stage will be compensated by a gain change of the RGB control circuit. Pin 55 (BLKIN) of the UOC is used as the feedback input from the CRT base panel.
- **Blue stretch.** This function increases the color temperature of the bright scenes (amplitudes which exceed a value of 80% of the nominal amplitude). This effect is obtained by decreasing the small signal gain of the red and green channel signals, which exceed this 80% level.
- **Beam current limiting.** A beam current limiting circuit inside the UOC handles the contrast and brightness control for the RGB signals. This prevents the CRT from being overdriven, which could otherwise cause serious damage in the line output stage. The reference used for this purpose is the DC voltage on pin 54 (BLCIN) of the TV processor. Contrast and brightness reduction of the RGB output signals is therefore proportional to the voltage present on this pin. Contrast reduction starts when the voltage on pin 54 is lower than 2.8 V. Brightness reduction starts when the voltage on pin 54 is less than 1.7 V. The voltage on pin 54 is normally 3.3 V (limiter not active). During set switch-off, the black current control circuit generates a fixed beam current of 1 mA. This current ensures that the picture tube capacitance is discharged. During the switch-off period, the vertical deflection is placed in an over-scan position, so that the discharge is not visible on the screen.

RGB Amplifier

From outputs 56, 57, and 58 of IC 7200 the RGB signals are applied to the integrated output amplifier (7330) on the CRT panel. Via the outputs 7, 8, and 9, the picture tube cathodes are driven.

The supply voltage for the amplifier is +200 V and is derived from the line output stage.

SCAVEM (if present)

The SCAn VELOCITY Modulation (SCAVEM) circuitry is implemented in the layout of the picture tube panel. It is thus not an extra module. This circuit influences the horizontal deflection as a function of the picture content. In an ideal square wave, the sides are limited in slope due to a limited bandwidth (5 MHz). SCAVEM will improve the slope as follows:

- **At a positive slope** , a SCAVEM current is generated which supports the deflection current. At the first half of the slope, the spot is accelerated and the picture is darker. At the second half of the slope, the spot is delayed and the slope becomes steeper.
- **At the end of the slope** , the SCAVEM-current decays to zero and the spot is at the original position. An overshoot occurs which improves the impression of sharpness.
- **At the negative slope** , the SCAVEM-current counteracts the deflection. During the first half of the slope, the spot is delayed and the slope becomes steeper. During the second half the spot accelerates, the SCAVEM-current is zero at the end of the slope.

The R/G/B signals are fed into the SCAVEM circuit and differentiated by C2364/2365/2366 and the input impedance of 7360 stage. Diode 6364 (Schottky diode) is the coring component, which blocks all the signals below 0.3 V so that the noise is not amplified and all the signals larger than 0.3V are differentiated and amplified.

After differentiation, the signal is amplified by Q7360 with 3369 as the collector resistor. The biasing of the 7360 stage is done by 3369, 3361, 3360, 3362, and 3363.

Items 6367, 2367, 3367, 3361, and 2360 work as the clipping components that limit the SCAVEM current at a certain level, to prevent SCAVEM over correction.

After being buffered by 7369, the differentiated signals are coupled through 2375 and 2380 to the output stage. The output stage is configured into cascode stage and push-pull operation. The biasing is done by 3373, 3375, 3376, 3380, 3381, 3383, 3374, and 3384. The working voltage of the transistors is settled at half the supply voltage.

At the rising portion of the R/G/B signals, cascode 7380 and 7382 will be operating and will pull the current through the SCAVEM coil. Contrarily, at the falling portion of the R/G/B signals, cascode 7373 and 7366 will be operating and will push the current through the SCAVEM coil.

The capacitors 2362, 2373, and 2381 ground the high frequencies, to prevent high frequency amplification. The ferrite bead 5376 is for EMC purpose. Resistors 3374 and 3384 determine the output SCAVEM current.

Items 2378 and 3378 are for the fine-tuning for different SCAVEM coil impedances. They also help to suppress high frequency oscillation. Capacitor 2369 helps to suppress the high frequency components and also controls the SCAVEM delay.

Synchronization

Inside IC 7200 part D, the vertical and horizontal sync pulses are separated. These 'H' and 'V' signals are synchronized with the incoming CVBS signal. They are then fed to the H- and V-drive circuits and to the OSD/TXT circuit for synchronization of the On Screen Display and Teletext (CC) information.

Deflection

Horizontal Drive

The horizontal drive signal is obtained from an internal VCO, which is running at twice the line frequency. This frequency is divided by two, to lock the first control loop to the incoming signal.

When the IC is switched 'on', the 'Hdrive' signal is suppressed until the frequency is correct. The 'Hdrive' signal is available at pin 30. The 'Hflybk' signal is fed to pin 31 to phase lock the horizontal oscillator, so that Q7462 cannot switch 'on' during the flyback time.

The 'EWdrive' signal for the E/W circuit (if present) is available on pin 15, where it drives transistor 7400 to make linearity corrections in the horizontal drive.

When the set is switched on, the '+8V' voltage goes to pin 9 of IC 7200. The horizontal drive starts up in a soft start mode. It starts with a very short TON time of the horizontal output transistor. The TOFF of the transistor is identical to the time in normal operation. The starting frequency during switch on is therefore about 2 times higher than the normal value. The 'on' time is slowly increased to the nominal value in 1175 ms. When the nominal value is reached, the PLL is closed in such a way that only very small phase corrections are necessary.

The 'EHTinformation' line on pin 11 is intended to be used as a 'X-ray' protection. When this protection is activated (when the voltage exceeds 6 V), the horizontal drive (pin 30) is switched 'off' immediately. If the 'H-drive' is stopped, pin 11 will become low again. Now the horizontal drive is again switched on via the slow start procedure.

The 'EHTinformation' line (Aquadag) is also fed back to the UOC IC 7200 pin 54, to adjust the picture level in order to compensate for changes in the beam current.

The filament voltage is monitored for 'no' or 'excessive' voltage. This voltage is rectified by diode 6447 and fed to the emitter of transistor 7443. If this voltage goes above 6.8 V, transistor 7443 will conduct, making the 'EHT0' line 'high'. This will immediately switch off the horizontal drive (pin 30) via the slow stop procedure.

The horizontal drive signal exits IC 7200 at pin 30 and goes to 7462, the horizontal driver transistor. The signal is amplified and coupled to the base circuit of 7460, the horizontal output transistor. This will drive the line output transformer (LOT) and associated circuit. The LOT provides the extra high voltage (EHT), the VG2 voltage and the focus and filament voltages for the CRT, while the line output circuit drives the horizontal deflection coil.

Vertical Drive

A divider circuit performs the vertical synchronization. The vertical ramp generator needs an external resistor (R3245, pin 20) and capacitor (C2244, pin 21). A differential output is available at pins 16 and 17, which are DC-coupled with the vertical output stage.

During the insertion of RGB signals, the maximum vertical frequency is increased to 72 Hz so that the circuit can also synchronize on signals with a higher vertical frequency like VGA. To avoid damage of the picture tube when the vertical deflection fails, the guard output is fed to the beam current limiting input. When a failure is detected, the RGB-outputs are blanked. When no vertical deflection output stage is connected, this guard circuit will also blank the output signals.

These 'V_DRIVE+' and 'V_DRIVE-' signals are applied to the input pins 1 and 2 of IC 7471 (full bridge vertical deflection amplifier). These are voltage driven differential inputs. As the driver device (IC 7200) delivers output currents, R3474 and R3475 convert them to voltage. The differential input voltage is compared with the voltage across measuring resistor R3471 that provides internal feedback information. The voltage across this measuring resistor is proportional to the output current, which is available at pins 4 and 7 where they drive the vertical deflection coil (connector 0222) in phase opposition.

IC 7471 is supplied by +13 V. The vertical flyback voltage is determined by an external supply voltage at pin 6 (VlotAux+50V). This voltage is almost totally available as flyback voltage across the coil, this being possible due to the absence of a coupling capacitor (which is not necessary, due to the 'bridge' configuration).

Deflection Corrections

The Linearity Correction

A constant voltage on the horizontal deflection coil should result in a sawtooth current. This however is not the case as the resistance of the coil is not negligible. In order to compensate for this resistance, a pre-magnetized coil L5457 is used. R3485 and C2459 ensure that L5457 does not excite, because of its own parasite capacitance. This L5457 is called the 'linearity coil'.

The Mannheim Effect

When clear white lines are displayed, the high-voltage circuit is heavily loaded. During the first half of the flyback, the high voltage capacitors are considerable charged. At that point in time, the deflection coil excites through C2465. This current peak, through the high-voltage capacitor, distorts the flyback pulse. This causes synchronization errors, causing an oscillation under the white line.

During $t_3 - t_5$, C2490//2458 is charged via R3459. At the moment of the flyback, C2490//2458 is subjected to the negative voltage pulses of the parabola as a result of which D6465 and D6466 are conducting and C2490//2458 is switched in parallel with C2456//2457. The high-voltage diodes are conducting this moment. Now extra energy is

available for excitation through C2465 and the line deflection. Consequently, the flyback pulse is less distorted.

The S-Correction

Since the sides of the picture are further away from the point of deflection than from the center, a linear sawtooth current would result in a non-linear image being scanned (the center would be scanned slower than the sides). For the center-horizontal line, the difference in relation of the distances is larger than those for the top and bottom lines. An S-shaped current will have to be superimposed onto the sawtooth current. This correction is called finger-length correction or S-correction.

C2456//2457 is relatively small, as a result of which the sawtooth current will generate a parabolic voltage with negative voltage peaks. Left and right, the voltage across the deflection coil decreases, and the deflection will slow down; in the center, the voltage increases and deflection is faster. The larger the picture width, the higher the deflection current through C2456//2457. The current also results in a parabolic voltage across C2484//2469, resulting in the finger length correction proportionally increasing with the picture width. The east/west drive signal will ensure the largest picture width in the center of the frame. Here the largest correction is applied.

East/West Correction

In this chassis, there are three types of CRTs, namely the 100°, 110° and wide screen CRTs. The 100° CRT is raster-correction-free and does not need East/West correction. The 110° 4:3 CRT comes with East/West correction and East/West protection. The wide screen TV sets have all the correction of the 110 4:3 CRT and also have additional picture format like the 4:3 format, 16:9, 14:9, 16:9 zoom, subtitle zoom and the Super-Wide picture format

A line, written at the upper- or lower side of the screen, will be larger at the screen center when a fixed deflection current is used. Therefore, the amplitude of the deflection current must be increased when the spot approaches the center of the screen. This is called the East/West or pincushion correction.

The 'Ewdrive' signal from pin 15 of IC 7200 takes care for the correct correction. It drives FET 7400. It also corrects breathing of the picture, due to beam current variations (the EHT varies dependent of the beam current). This correction is derived from the 'EHTinformation' line.

Two protections are built-in for the E/W circuit: over-current and over-voltage protection. See paragraph 9.7.6.

Panorama

The panorama function is only used in 16:9 sets. This is a function to enable the 4:3 and Super-Wide feature. It drives the 'Bass_panorama' line, to activate relay 1400. When this

relay is switched on, the capacitors 2453//2454 are added in parallel to the default S-correction capacitors 2456//2457. This results in an increased capacitance, a lower resonance frequency of the line deflection coil and the S-correction capacitors and therefore a less steep S-corrected line deflection current.

Power Supply

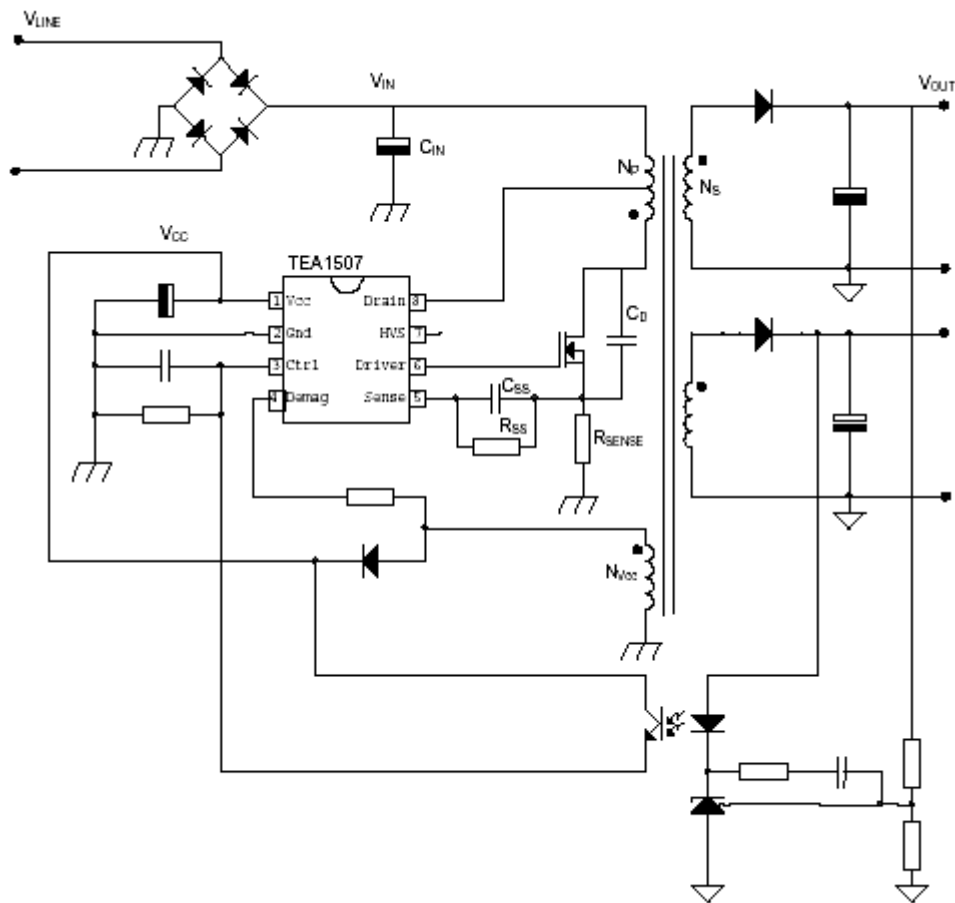


Figure: Switched Mode Power Supply standard circuit

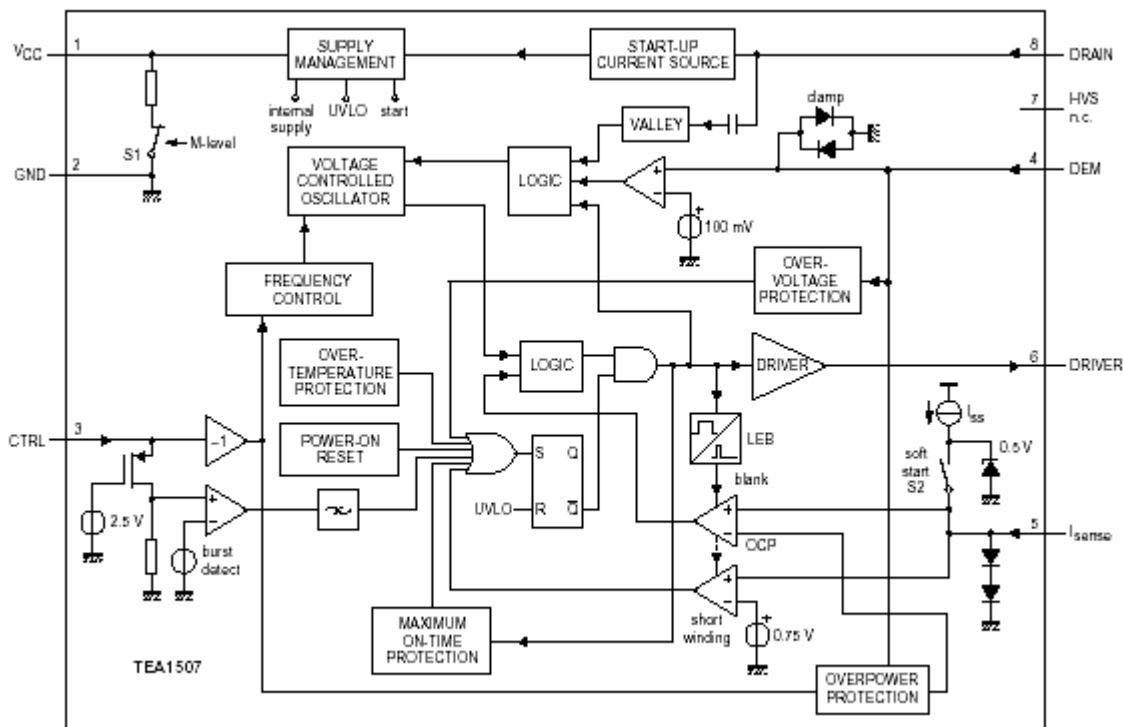


Figure: Internal blockdiagram of the driver IC (TEA1507)

Introduction

The supply is a Switching Mode Power Supply (SMPS). The frequency of operation varies with the circuit load. This 'Quasi-Resonant Flyback' behavior has some important benefits compared to a 'hard switching' fixed frequency Flyback converter. The efficiency can be improved up to 90%, which results in lower power consumption. Moreover, the supply runs cooler and safety is enhanced.

The power supply starts operating when a DC voltage goes from the rectifier bridge via T5520, R3532 to pin 8. The operating voltage for the driver circuit is also taken from the 'hot' side of this transformer.

The switching regulator IC 7520 starts switching the FET 'on' and 'off', to control the current flow through the primary winding of transformer 5520. The energy stored in the primary winding during the 'on' time is delivered to the secondary windings during the 'off' time.

The 'MainSupply' line is the reference voltage for the power supply. It is sampled by resistors 3543 and 3544 and fed to the input of the regulator 7540 / 6540. This regulator drives the feedback optocoupler 7515 to set the feedback control voltage on pin 3 of 7520. The power supply in the set is 'on' any time AC power goes to the set.

Derived Voltages

The voltages supplied by the secondary windings of T5520 are:

- 'MainAux' for the audio circuit (voltage depends on set execution, see table below),
- 3.3 V and 3.9 V for the microprocessor and
- 'MainSupply' for the horizontal output (voltage depends on set execution, see table below).

Other supply voltages are provided by the LOT. It supplies +50 V (only for large screen sets), +13 V, +8 V, +5 V, and a +200 V source for the video drive. The secondary voltages of the LOT are monitored by the 'EHTinformation' lines. These lines are fed to the video processor part of the UOC IC 7200 on pins 11 and 34.

This circuit will shut 'off' the horizontal drive in case of over-voltage or excessive beam current.

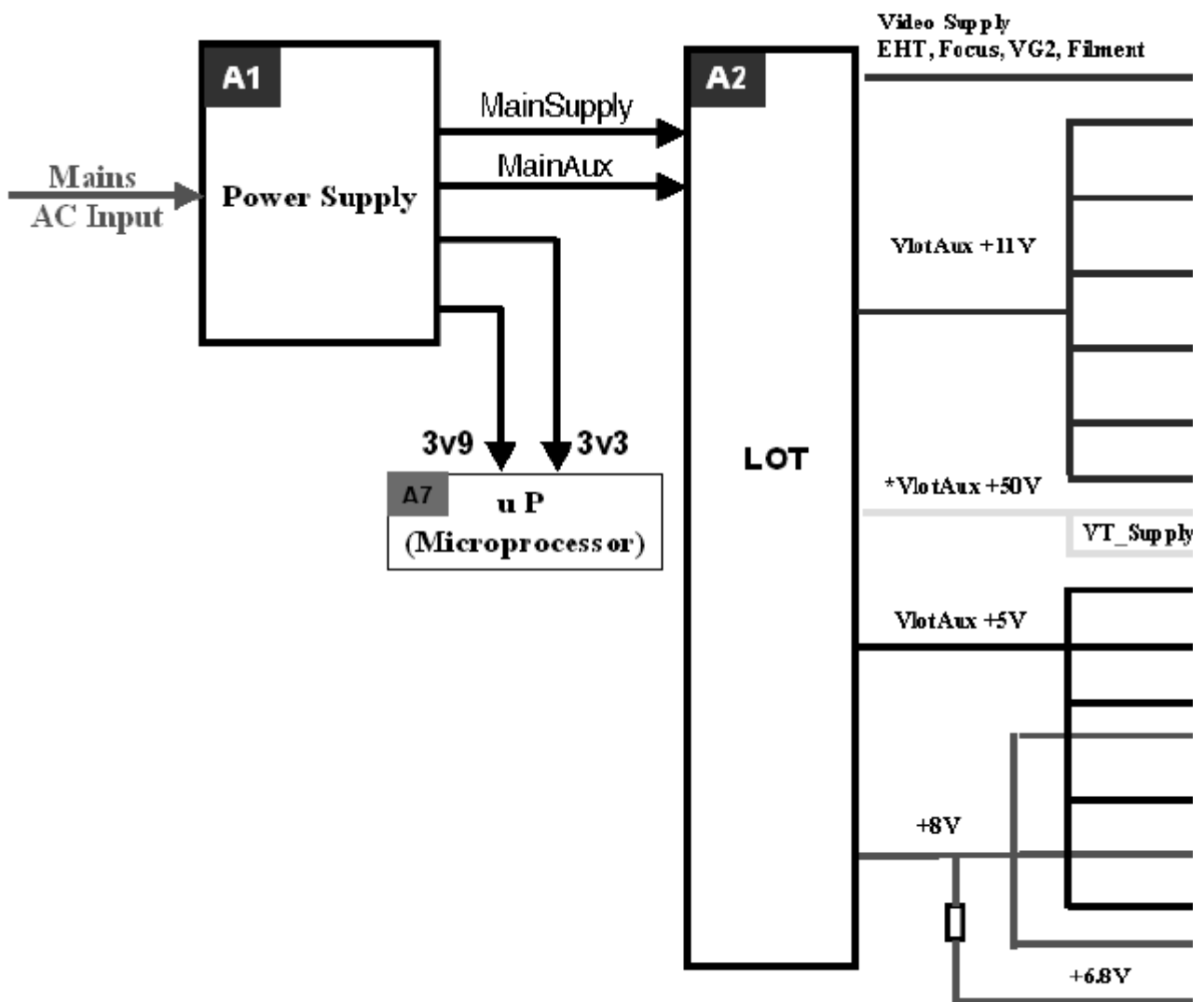


Figure: Derived voltages

Degaussing

When the set is switched on, the degaussing relay 1515 is immediately activated as transistor 7580 is conducting. Due to the RC-time of R3580 and C2580, it will last about 3 to 4 seconds before transistor 7580 is switched off.

Basic IC Functionality

For a clear understanding of the Quasi-Resonant behavior, it is possible to explain it by a simplified circuit diagram (see Figure below). In this circuit diagram, the secondary side is transferred to the primary side and the transformer is replaced by an inductance L_P . C_D is the total drain capacitance including the resonance capacitor C_R , parasitic output capacitor C_{OSS} of the MOSFET and the winding capacitance C_W of the transformer. The turn ratio of the transformer is represented by n (N_P/N_S).

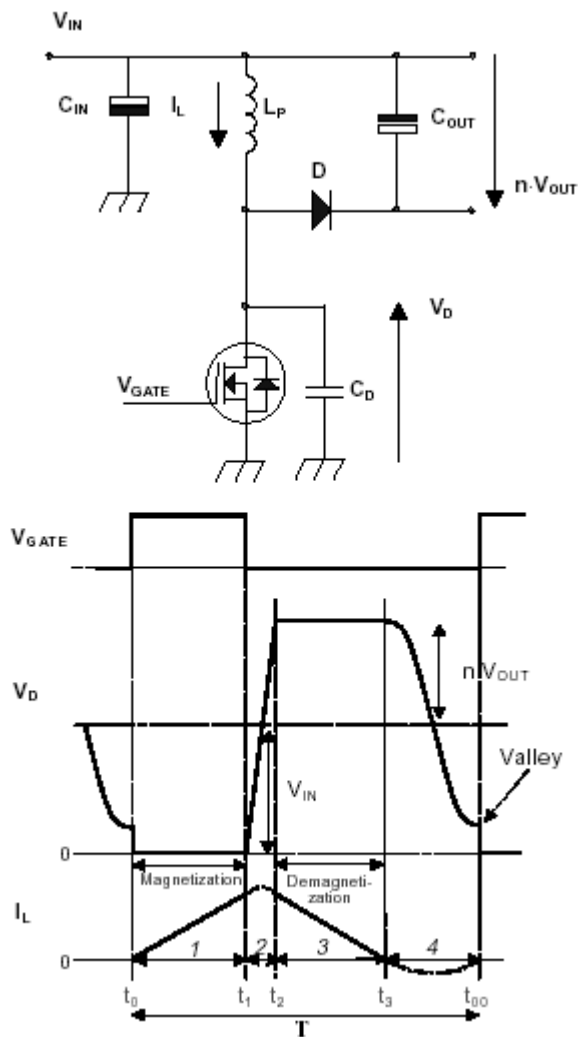


Figure: QR-mode time intervals

In the Quasi-Resonant mode each period can be divided into four different time intervals, in chronological order:

- **Interval 1: $t_0 < t < t_1$ primary stroke.** At the beginning of the first interval, the MOSFET is switched 'on' and energy is stored in the primary inductance (magnetization). At the end, the MOSFET is switched 'off' and the second interval starts.
- **Interval 2: $t_1 < t < t_2$ commutation time.** In the second interval, the drain voltage will rise from almost zero to $V_{IN} + n \cdot (V_{OUT} + V_F)$. V_F is the forward voltage drop of the diode that will be omitted from the equations from now on. The current will change its positive derivative, corresponding to V_{IN} / L_P , to a negative derivative, corresponding to $-n \cdot V_{OUT} / L_P$.
- **Interval 3: $t_2 < t < t_3$ secondary stroke.** In the third interval, the stored energy is transferred to the output, so the diode starts to conduct and the inductive current I_L will decrease. In other words, the transformer will be demagnetized. When the inductive current has become zero the next interval begins.
- **Interval 4: $t_3 < t < t_0$ resonance time.** In the fourth interval, the energy stored in the drain capacitor C_D will start to resonate with the inductance L_P . The voltage and current waveforms are sinusoidal waveforms. The drain voltage will drop from $V_{IN} + n \cdot V_{OUT}$ to $V_{IN} - n \cdot V_{OUT}$.

Frequency Behavior

The frequency in the QR-mode is determined by the power stage and is not influenced by the controller (important parameters are L_P and C_D). The frequency varies with the input voltage V_{IN} and the output power P_{OUT} . If the required output power increases, more energy has to be stored in the transformer. This leads to longer magnetizing t_{PRIM} and demagnetizing t_{SEC} times, which will decrease the frequency. See the frequency versus output power characteristics below. The frequency characteristic is not only output power-, but also input voltage dependent. The higher the input voltage, the smaller t_{PRIM} , so the higher the frequency will be.

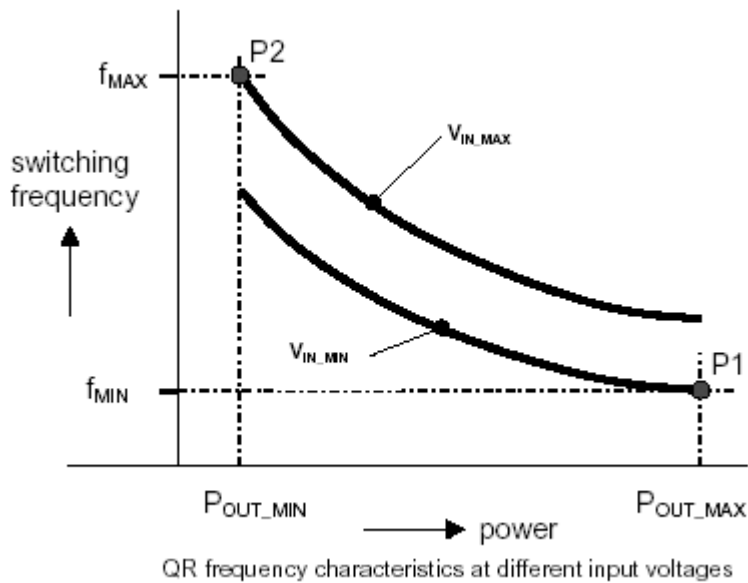


Figure: QR frequency behaviour

Point P1 is the minimum frequency f_{MIN} that occurs at the specified minimum input voltage and maximum output power required by the application. Of course the minimum frequency has to be chosen above the audible limit (>20 kHz).

Start-Up Sequence

When the rectified AC voltage V_{IN} (via the center tap connected to pin 8) reaches the Mains dependent operation level (Mlevel: between 60 and 100 V), the internal 'Mlevel switch' will be opened and the start-up current source is enabled to charge capacitor C2521 at the V_{CC} pin as shown below.

The 'soft start' switch is closed when the V_{CC} reaches a level of 7 V and the 'soft start' capacitor C_{SS} (C2522, between pin 5 and the sense resistor R3526), is charged to 0.5 V. Once the V_{CC} capacitor is charged to the start-up voltage $V_{\text{CC}}\text{-start}$ (11 V), the IC starts driving the MOSFET. Both internal current sources are switched 'off' after reaching this start-up voltage. Resistor R_{SS} (3524) will discharge the 'soft start' capacitor, such that the peak current will slowly increase. This to prevent 'transformer rattle'. During start-up, the V_{CC} capacitor will be discharged until the moment that the primary auxiliary winding takes over this voltage.

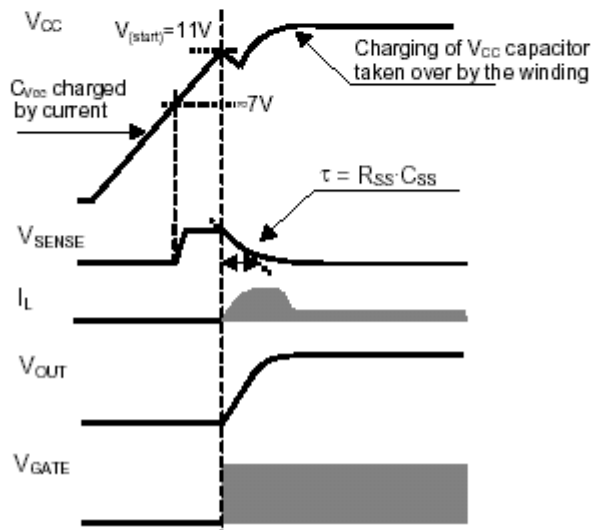
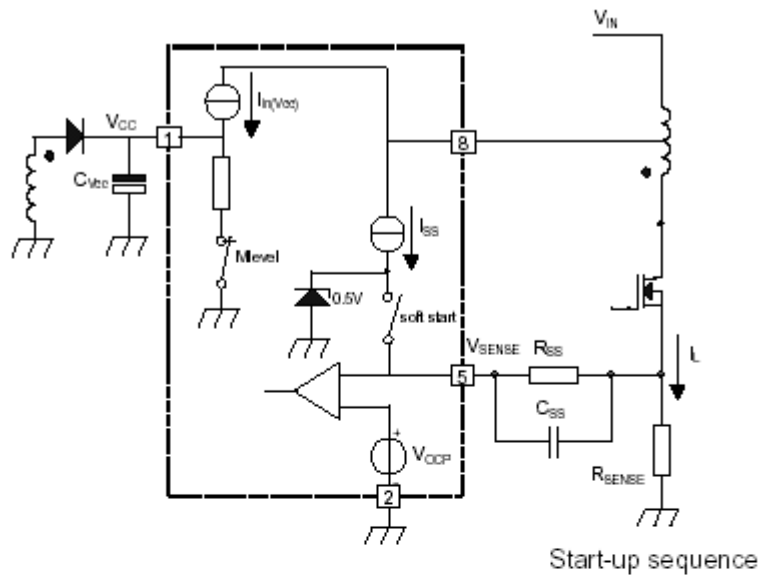


Figure: Start-up behaviour

The moment that the voltage on pin 1 drops below the 'under voltage lock out' level (UVLO = ± 9 V), the IC will stop switching and will enter a safe restart from the rectified mains voltage.

Operation

The supply can run in three different modes depending on the output power:

- **Quasi-Resonant mode (QR).** The 'QR' mode, described above, is used during normal operation. This will give a high efficiency.
- **Frequency Reduction mode (FR).** The 'FR' mode (also called 'VCO' mode) is implemented to decrease the switching losses at low output loads. In this way, the efficiency at low output powers is increased, which enables power consumption smaller than 3 W during stand-by. The voltage at the pin 3 (Ctrl) determines where

the frequency reduction starts. An external Ctrl voltage of 1.425 V corresponds with an internal VCO level of 75 mV. This fixed VCO level is called $V_{VCO,start}$. The frequency will be reduced in relation to the VCO voltage between 75 mV and 50 mV (at levels larger than 75 mV, Ctrl voltage < 1.425V, the oscillator will run on maximum frequency $f_{oscH} = 175$ kHz typically). At 50 mV ($V_{VCO,max}$), the frequency is reduced to the minimum level of 6 kHz. Valley switching is still active in this mode.

- **Minimum Frequency mode (MinF).** At VCO levels below 50 mV, the minimum frequency will remain on 6 kHz, which is called the 'MinF' mode. Because of this low frequency, it is possible to run at very low loads without having any output regulation problems.

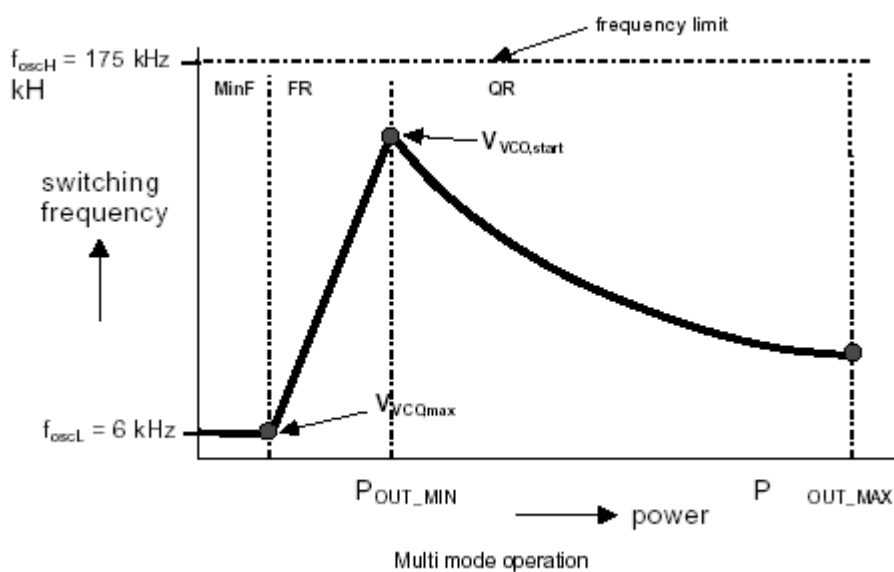


Figure: Different supply modes

Safe-Restart Mode

This mode is introduced to prevent the components from being destroyed during eventual system fault conditions. It is also used for the Burst mode. The Safe-Restart mode will be entered if it is triggered by one of the following functions:

- Over voltage protection,
- Short winding protection,
- Maximum 'on time' protection,
- V_{CC} reaching UVLO level (fold back during overload),
- Detecting a pulse for Burst mode,
- Over temperature protection.

When entering the Safe-Restart mode, the output driver is immediately disabled and latched. The V_{CC} winding will not charge the VCC capacitor anymore and the V_{CC} voltage will drop until UVLO is reached. To recharge the V_{CC} capacitor, the internal current source ($I_{(restart)(VCC)}$) will be switched 'on' to initiate a new start-up sequence as described before. This Safe-Restart mode will persist until the controller detects no faults or burst triggers.

Standby

The set goes to Standby in the following cases:

- After pressing the 'standby' key on the remote control.
- When the set is in protection mode.

In Standby, the power supply works in 'burst mode'. Burst mode can be used to reduce the power consumption below 1 W at stand-by. During this mode, the controller is active (generating gate pulses) for only a short time and for a longer time inactive waiting for the next burst cycle.

In the active period, the energy is transferred to the secondary and stored in the buffer capacitor C_{STAB} in front of the linear stabilizer (see Figure below). During the inactive period, the load (e.g. microprocessor) discharges this capacitor. In this mode, the controller makes use of the Safe-Restart mode.

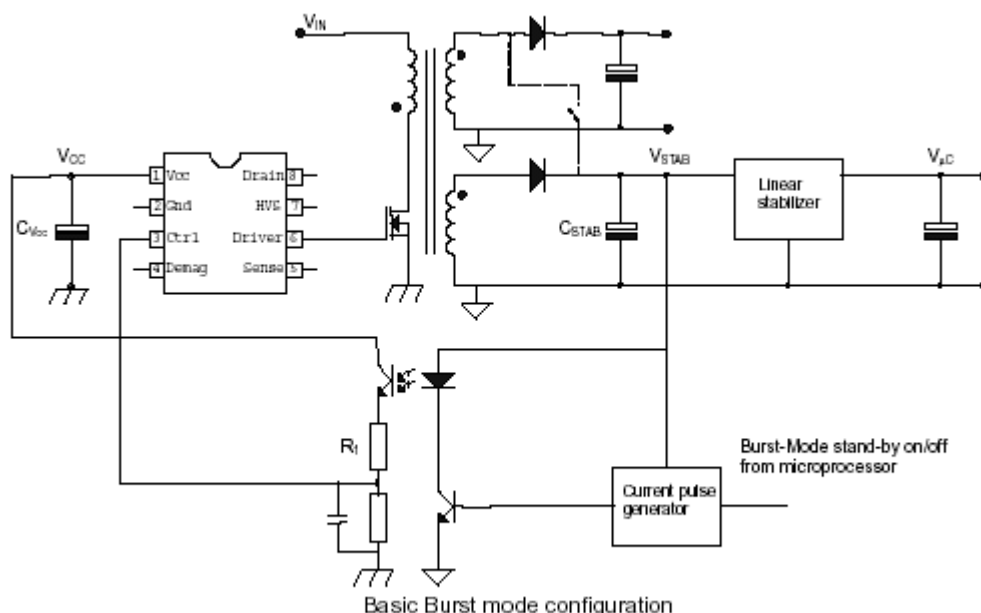


Figure: Supply standby mode (burst mode)

The system enters burst mode standby when the microprocessor activates the 'Stdbby_con' line. When this line is pulled high, the base of Q7541 is allowed to go high. This is triggered by the current from collector Q7542. When Q7541 turns 'on', the opto-coupler (7515) is activated, sending a large current signal to pin 3 (Ctrl). In response to this signal, the IC stops switching and enters a 'hiccup' mode. This burst activation signal should be present for longer than the 'burst blank' period (typically 30 s): the blanking time prevents false burst triggering due to spikes.

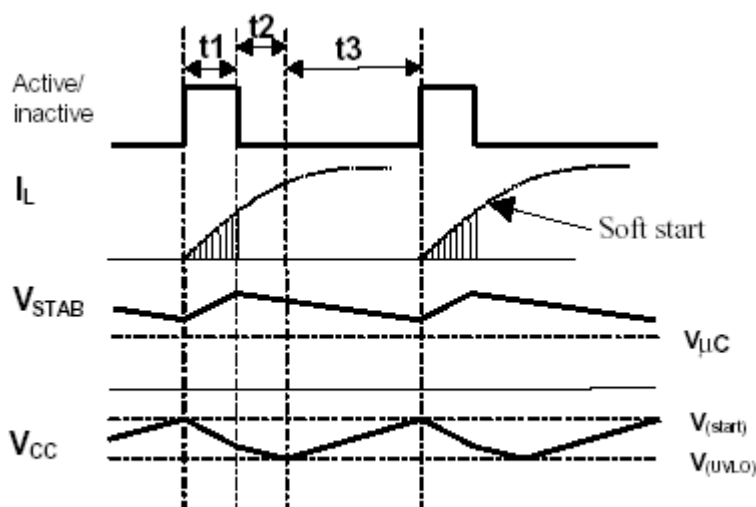
Burst mode standby operation continues until the microcontroller pulls the 'Stdbby_con' signal low again. The base of Q7541 is unable to go high, thus cannot turn 'on'. This will disable the burst mode. The system then enters the start-up sequence and begins normal switching behavior.

For a more detailed description of one burst cycle, three time intervals are defined:

t1: Discharge of V_{CC} when gate drive is active. During the first interval, energy is transferred, which result in a ramp-up of the output voltage (V_{STAB}) in front of the stabilizer. When enough energy is stored in the capacitor, the IC will be switched 'off' by a current pulse generated at the secondary side. This pulse is transferred to the primary side via the opto coupler. The controller will disable the output driver (safe restart mode) when the current pulse reaches a threshold level of 16 mA into the Ctrl pin. A resistor R1 (R3519) is placed in series with the opto coupler, to limit the current going into the Ctrl pin. Meanwhile the V_{CC} capacitor is discharged but has to stay above V_{UVLO} .

t2: Discharge of V_{CC} when gate drive is inactive. During the second interval, the V_{CC} is discharged to V_{UVLO} . The output voltage will decrease depending on the load.

t3: Charge of V_{CC} when gate drive is inactive. The third interval starts when the UVLO is reached. The internal current source charges the V_{CC} capacitor (also the soft start capacitor is recharged). Once the V_{CC} capacitor is charged to the start-up voltage, the driver is activated and a new burst cycle is started.



Burst mode waveforms

Figure: Burst mode waveforms

Protection Events

The SMPS IC 7520 has the following protection features:

Demagnetization sense

This feature guarantees discontinuous conduction mode operation in every situation. The oscillator will not start a new primary stroke until the secondary stroke has ended. This is to ensure that FET 7521 will not turn on until the demagnetization of transformer 5520 is complete. The function is an additional protection feature against:

- saturation of the transformer,
- damage of the components during initial start-up,
- an overload of the output.

The demag(netization) sense is realized by an internal circuit that guards the voltage (V_{demag}) at pin 4 that is connected to V_{CC} winding by resistor R_1 (R3522).

The Figure below shows the circuit and the idealized waveforms across this winding.

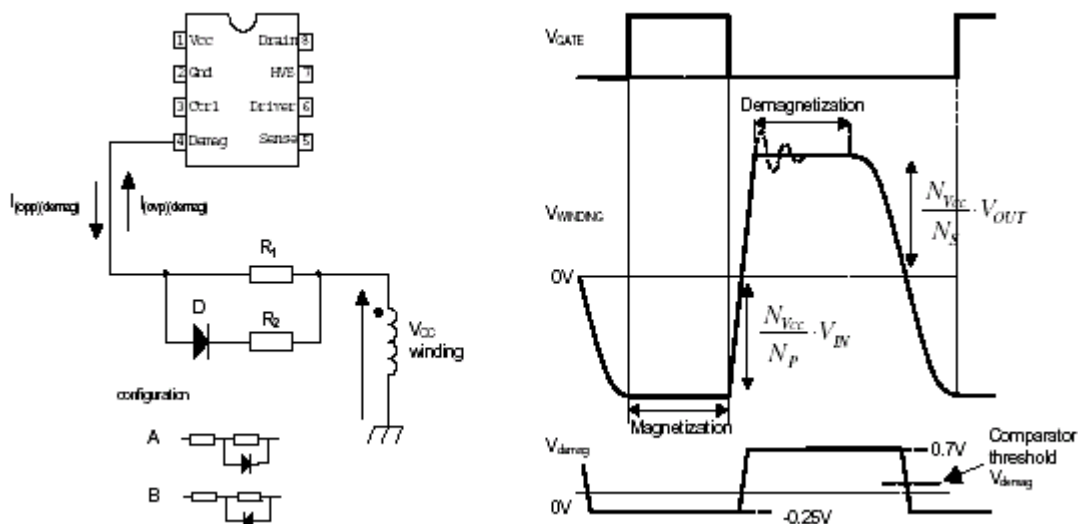


Figure: Demagnetisation protection

Over Voltage Protection

The Over Voltage Protection ensures that the output voltage will remain below an adjustable level. This works by sensing the auxiliary voltage via the current flowing into pin 4 (DEM) during the secondary stroke. This voltage is a well-defined replica of the output voltage. Any voltage spikes are averaged by an internal filter.

If the output voltage exceeds the OVP trip level, the OVP circuit switches the power MOSFET 'off'.

Next, the controller waits until the 'under voltage lock out' level ($UVLO = \pm 9\text{ V}$) is reached on pin 1 (V_{CC}). This is followed by a safe restart cycle, after which switching starts again.

This process is repeated as long as the OVP condition exists. The output voltage at which the OVP function trips, is set by the demagnetization resistor R3522.

Over Current Protection

The internal OCP protection circuit limits the 'sense' voltage on pin 5 to an internal level.

Over Power Protection

During the primary stroke, the rectified AC input voltage is measured by sensing the current drawn from pin 4 (DEM). This current is dependent on the voltage on pin 9 of transformer 5520 and the value of R3522. The current information is used to adjust the peak drain current, which is measured via pin I_{SENSE} .

Short Winding Protection

If the 'sense' voltage on pin 5 exceeds the short winding protection voltage (0.75 V), the converter will stop switching. Once V_{CC} drops below the UVLO level, capacitor C2521 will be recharged and the supply will start again. This cycle will be repeated until the short circuit is removed (safe restart mode).

The short winding protection will also protect in case of a secondary diode short circuit. This protection circuit is activated after the leading edge blanking time (LEB).

LEB time

The LEB (Leading Edge Blanking) time is an internally fixed delay, preventing false triggering of the comparator due to current spikes. This delay determines the minimum 'on' time of the controller.

Over Temperature protection

When the junction temperature exceeds the thermal shutdown temperature (typ. 140° C), the IC will disable the driver. When the V_{CC} voltage drops to UVLO, the V_{CC} capacitor will be recharged to the $V(\text{start})$ level. If the temperature is still too high, the V_{CC} voltage will drop again to the UVLO level (Safe-Restart mode). This mode will persist until the junction temperature drops 8 degrees typically below the shutdown temperature.

Mains dependent operation enabling level

To prevent the supply from starting at a low input voltage, which could cause audible noise, a mains detection is implemented (Mlevel). This detection is provided via pin 8, which detects the minimum start-up voltage between 60 and 100 V. As previous mentioned, the controller is enabled between 60 and 100 V.

An additional advantage of this function is the protection against a disconnected buffer capacitor (C_{IN}). In this case, the supply will not be able to start-up because the V_{CC} capacitor will not be charged to the start-up voltage.

Control

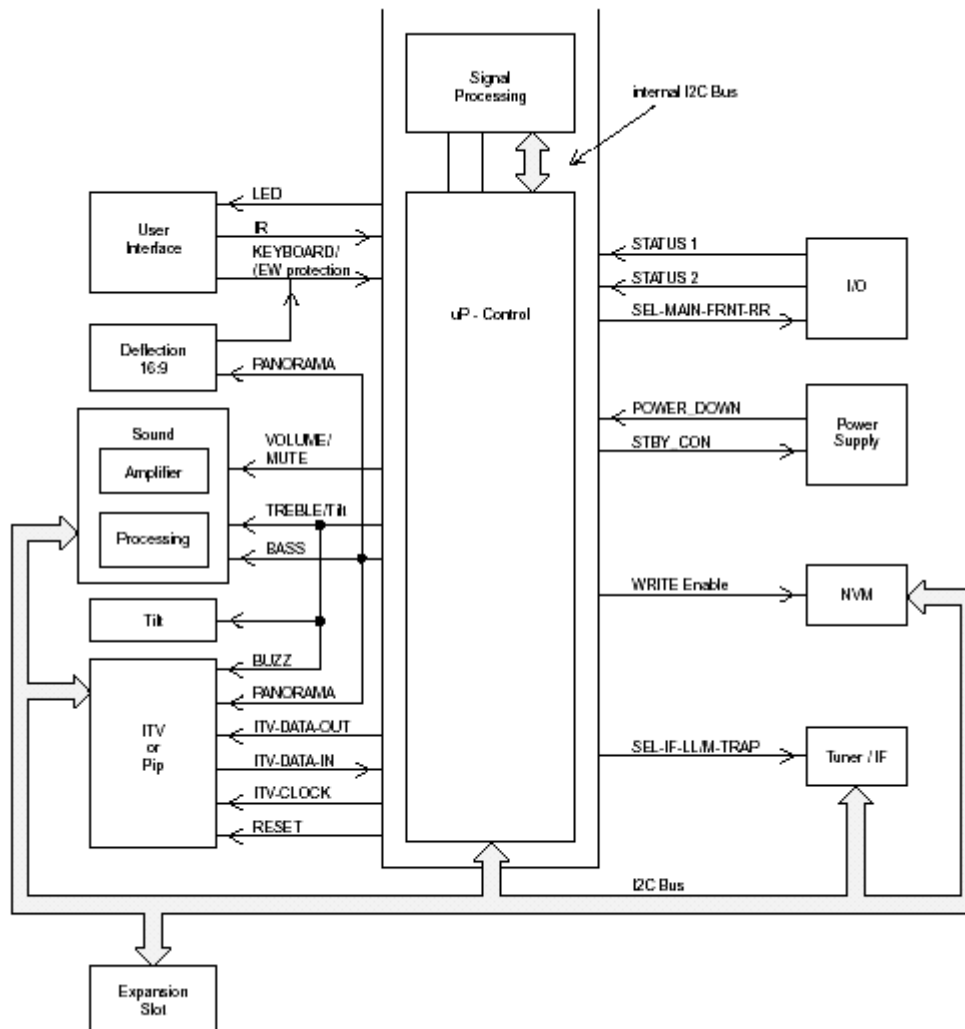


Figure: Block diagram set control

Introduction

The microprocessor part of the UOC, has the complete control and teletext on board. User menu, Service Default Mode, Service Alignment Mode and Customer Service Mode are generated by the uP. Communication to other ICs is done via the I2C-bus.

I2C-Bus

The main control system, which consists of the microprocessor part of the UOC (7200), is linked to the external devices (tuner, NVM, MSP, etc) by means of the I2C-bus. An internal I2C-bus is used to control other signal processing functions, like video processing, sound IF, vision IF, synchronization, etc.

User Interface

The 'L01.1U AC' uses a remote control with RC5 protocol. The incoming signal is connected to pin 67 of the UOC.

The 'Top Control' keyboard, connected to UOC pin 80, can also control the set. Button recognition is done via a voltage divider.

The front LED (6691) is connected to an output control line of the microprocessor (pin 5). It is activated to provide the user information about whether or not the set is working correctly (e.g., responding to the remote control, normal operation (USA only) or fault condition)

In- and Output Selection

For the control of the input and output selections, there are three lines:

- **STATUS1.** This signal provides information to the microprocessor on whether a video signal is available on the SCART1 AV input and output port (only for Europe). This signal is not connected in NAFTA sets.
- **STATUS2.** This signal provides information to the microprocessor on whether a video signal is available on the SCART2 AV input and output port (only for Europe). For sets with an SVHS input it provides the additional information if a Y/C or CVBS source is present. The presence of an external Y/C source makes this line 'high' while a CVBS source makes the line 'low'.
- **SEL-MAIN-FRNT-RR.** This is the source select control signal from the microprocessor. This control line is under user control or can be activated by the other two control lines.

Power Supply Control

The microprocessor part is supplied with 3.3 V and 3.9 V both derived from the 'MainAux' voltage via a 3V3 stabilizer (7560) and a diode.

Two signals are used to control the power supply:

- **Stdbby_con.** This signal is generated by the microprocessor when over-current takes place at the 'MainAux' line. This is done to enable the power supply into standby burst mode, and to enable this mode during a protection. This signal is 'low' under normal operation conditions and goes to 'high' (3.3 V) under 'standby' and 'fault' conditions.
- **POWER_DOWN.** This signal is generated by the power supply. Under normal operating conditions, this signal is 'high' (3.3 V). During 'standby' mode, this signal is a pulse train of approx. 10 Hz and a 'high' duration of 5 ms. It is used to give information to the UOC about the fault condition in the Audio amplifier supply circuit. This information is generated by sensing the current on the 'MainAux' line (using voltage drop across R3564 to trigger Q7562). This signal goes 'low' when the DC-current on the 'MainAux' line exceeds 1.6 - 2.0 A. It is also used to give an early warning to the UOC about a power failure. Then the information is used to mute the sound amplifier to prevent a switch off noise and to solve the switch-off spot.

Protection Events

Several protection events are controlled by the UOC:

- **BC protection** , to protect the picture tube from a too high beam current. The UOC has the capability of measuring the normal back level current during the vertical flyback. So if for some reason the CRT circuit is malfunctioning (i.e. high beam current), the normal black current will be out of the 75 A range, and the UOC will trigger the power supply to shut down. However, this is a high beam-current situation, the TV screen will be bright white before the set is shut down.
- **E/W protection** , two protection mechanisms are built in, over-current and over-voltage.
 - In case of over-current due to defective parts in the line deflection output stage, a high current will flow through resistors 3405//3406. If this current is large enough to create a voltage drop of 0.7 V across 3405//3406, transistor Q7606 (in A7 diagram) will conduct and pin 80 of the UOC will be pulled down. Thereafter, the UOC will shut down the power supply. In case of further current increase, the fused resistor 3411 is built-in for double protection.
 - In case of a high voltage appearing across capacitor 2401 (dependent of the tube size), which is high enough to trigger zener diode 6401 into conduction, transistor Q7606 (in A7 diagram) will conduct and UOC is triggered to shut down the power supply.
- **I2C protection** , to check whether all I2C ICs are functioning.

In case one of these protections is activated, the set will go into 'standby'.

The 'on' and 'standby' LEDs are controlled via the UOC.

DVD Combi Interface Board

Introduction

The function of the DVD Combi Interface Board is to provide an interface between the SD3.x DVD module and the TV main chassis. It consists of a power supply circuit to provide some different voltages for the DVD module, and a pair of analog multiplexer/demultiplexers that are used to switch the audio and video signals between DVD and an external side AV source.

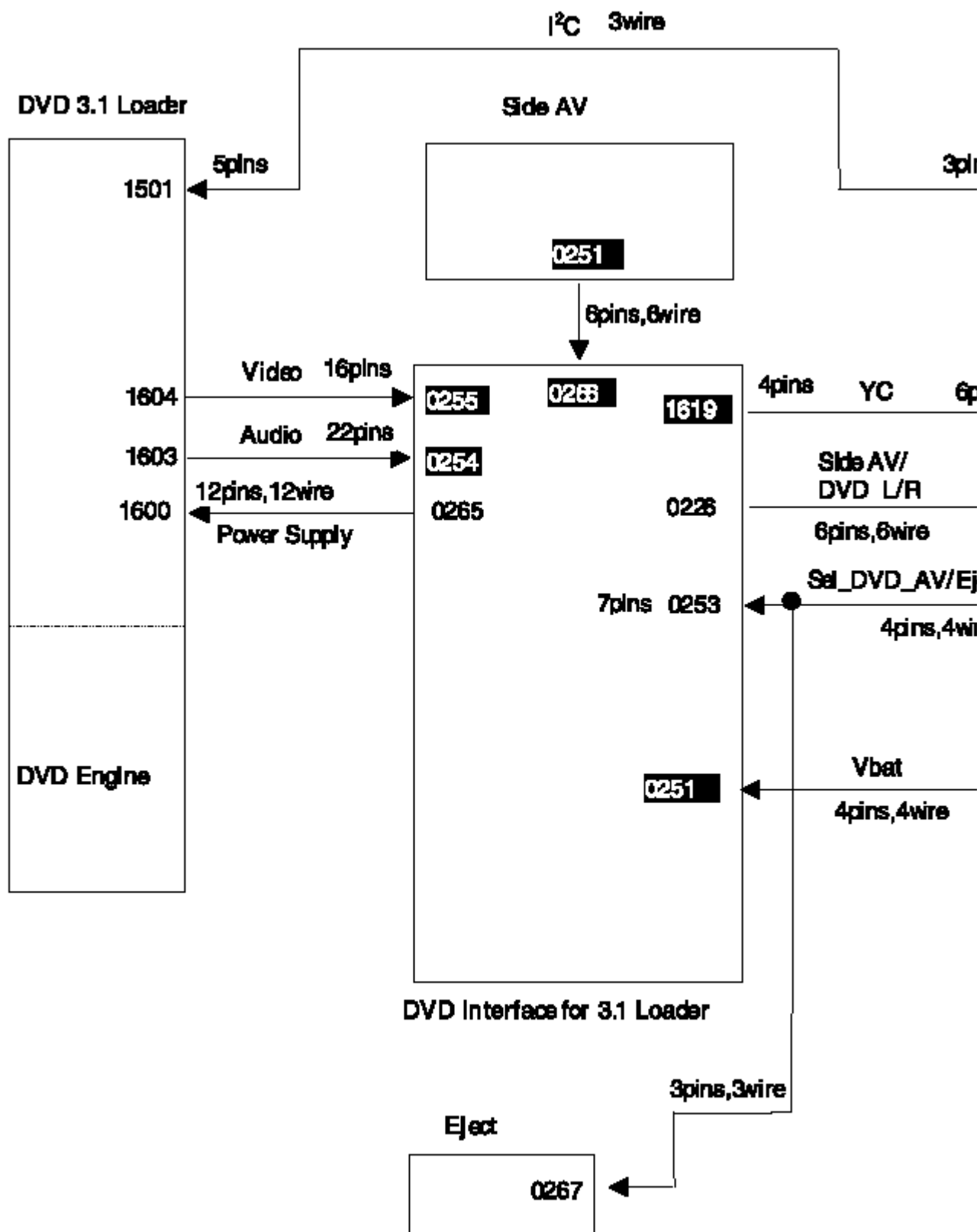


Figure: Interface block diagram (with Side I/O)

Switching Overview

Below you will find the switching Logic Table for sets without Side I/O.

Table: Switching Logic Table (Without Side I/O)

Mode	I/O Port		
	COMB-SEL-CVBSO-AV2	COMB-BYPASS	SEL-MAIN-FRNT-RR
RF	0	1	1
AV1	0	1	1
YUV	-	-	-
AV2	0	1	1
SVHS	0	1	1
DVD	0	0	0

2K3 Nafta/Latam DVD I/O Overview :-

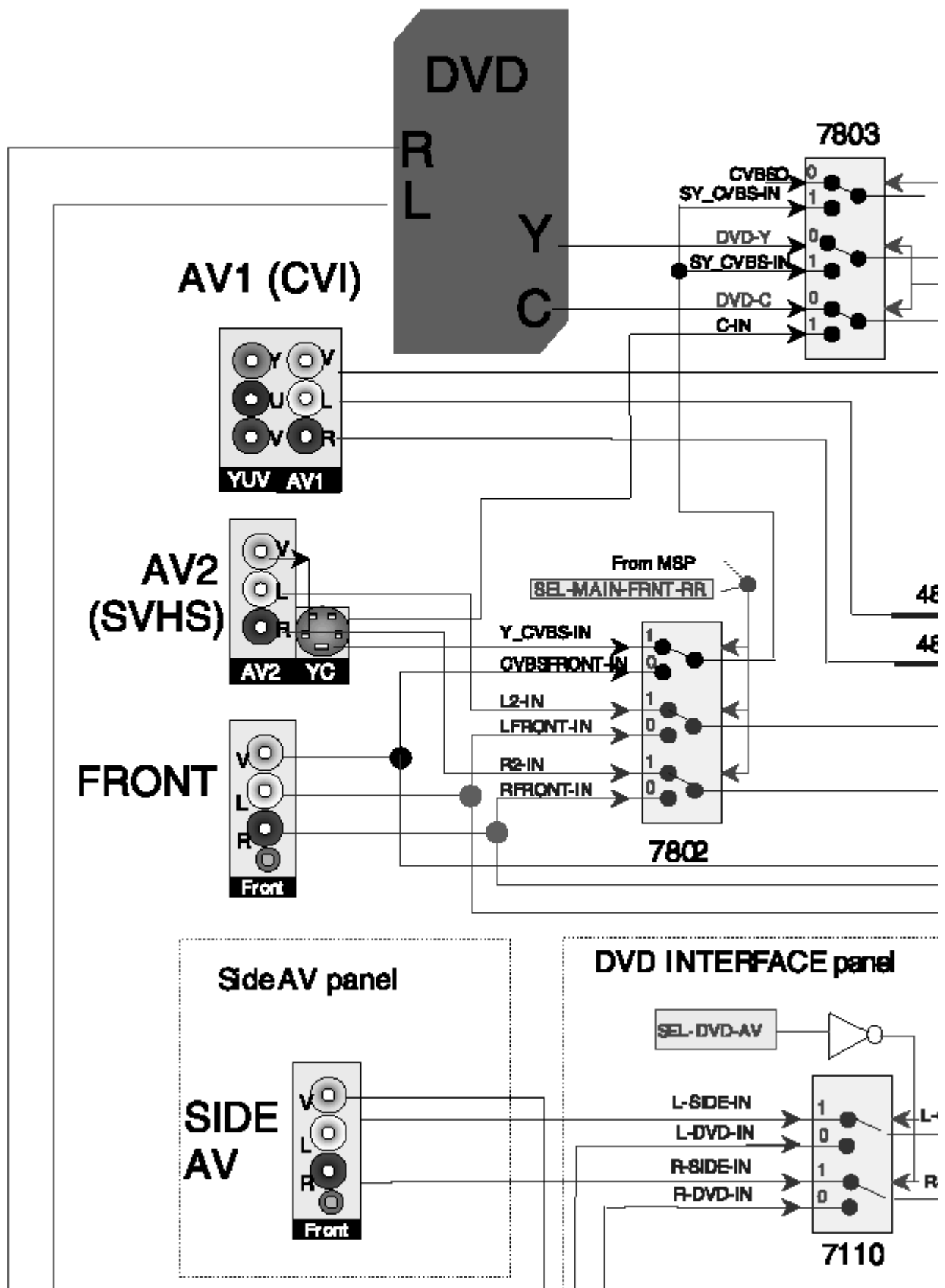


Figure: I/O switching overview (with Side I/O)

Below you will find the switching Logic Table for sets with Side I/O. See also figure 3 above.

Table: Switching Logic Table (With Side I/O)

Mode	I/O Port			
	COMB-SEL-CVBSO-AV2	COMB-BYPASS	SEL-MAIN-FRNT-RR	SEL-DVD-AV
RF	0	1	1	0
AV1	0	1	1	0
YUV	0	1	1	0
AV2	0	1	1	0
SVHS	0	1	1	0
Side AV	0	1	0	0
DVD	0	0	0	1

Control

The SD3.x DVD module is, as slave, directly controlled by the main microprocessor on the main board.

The UOC pins 71 (SCL) and 72 (SDA) control the DVD module via connector 0267.

I/O Ports Control

Overview

Table: I/O Ports Control

No	I/O Configured	UOC pin	Conn.-pin	Functions
				For DVD_SEL_AV used in

1	Push-Pull	74	0240-2	Interface board for switching.
2	Push-Pull	75	0240-3	For DVD Standby Control (500ms active high pulse)
3	High Impedance	76	0240-4	For Eject (detect Eject action through this pin, '1' to eject).

Eject Button

Pin 76 is configured as an input port for reading the status of the "Eject" Button. When pin 76 reads LOW, this means that the "Eject" button is not pressed. When the "Eject" button is pressed, it will read HIGH. So, pins 75 and 76 together with GND are used to control the open and close actions of the DVD tray.

This input port should be set LOW and then polled periodically (about every 200ms) to check for a key pressed.

Table: Eject Button

EJECT	Status
HIGH	EJECT button is pressed; an OPEN or CLOSE tray action must follow.
LOW	Eject button not pressed.

SEL_DVD_AV

Pin 74 of the UOC is configured as a Push-Pull output port, which controls the selection between DVD Audio/Video and the Side AV source. This Push-Pull output port is then converted to a logic level of 0 V and 12 V by a transistor, which controls the logic at the HEF-switch selection at 12 V via a pull-up resistor.

Table: SEL_DVD_AV

SEL_DVD_AV	Actions
HIGH	Side AV video and audio source.
LOW	Select DVD Left/Right Audio/Video.

DVD_POWER

Configured as an output port, this signal controls the DVD power supply ON/OFF.

Table: DVD_STDBY

DVD_STDBY	Actions
HIGH	DVD power supplies switch OFF.
LOW	DVD power supplies switch ON.

Service Protection

When the DVD module is removed from an L01 DVD Combi set (for service or tests), the set tries to start in DVD mode. To avoid this, you must place resistor 3614 on the Main Board.

Abbreviation list

Abbreviation	Description
2CS	2 Carrier (or Channel) Stereo
ACI	Automatic Channel Installation: algorithm that installs TV sets directly from cable network by means of a predefined TXT page
ADC	Analogue to Digital Converter
AFC	Automatic Frequency Control: control signal used to tune to the correct frequency
AFT	Automatic Fine Tuning
AGC	Automatic Gain Control: algorithm that controls the video input of the feature box
AM	Amplitude Modulation
AP	Asia Pacific
AR	Aspect Ratio: 4 by 3 or 16 by 9
ATS	Automatic Tuning System

AV	External Audio Video
AVL	Automatic Volume Level
BC-PROT	Beam Current Protection
BCL	Beam Current Limitation
B/G	Monochrome TV system. Sound carrier distance is 5.5 MHz
BLC-INFORMATION	Black current information
BTSC	Broadcast Television Standard Committee. Multiplex FM stereo sound system, originating from the USA and used e.g. in LATAM and AP-NTSC countries
B-TXT	Blue teletext
CBA	Circuit Board Assembly
CC	Closed Caption
ComPair	Computer aided rePair
CRT	Cathode Ray Tube or picture tube
CSM	Customer Service Mode
CTI	Color Transient Improvement: manipulates steepness of chroma transients
CVBS	Composite Video Blanking and Synchronization
DAC	Digital to Analogue Converter
DBE	Dynamic Bass Enhancement: extra low frequency amplification
DBX	Dynamic Bass Expander
D/K	Monochrome TV system. Sound carrier distance is 6.5 MHz
DFU	Direction For Use: description for the end user
DNR	Dynamic Noise Reduction
DSP	Digital Signal Processing
DST	Dealer Service Tool: special remote control designed for dealers to enter e.g. service mode
DVD	Digital Versatile Disc
EEPROM	Electrically Erasable and Programmable Read Only Memory

EHT	Extra High Tension
EHT-INFORMATION	Extra High Tension information
EU	Europe
EW	East West, related to horizontal deflection of the set
EXT	External (source), entering the set via SCART or Cinch
FBL	Fast Blanking: DC signal accompanying RGB signals
FILAMENT	Filament of CRT
FLASH	Flash memory
FM	Field Memory
FM	Frequency Modulation
HA	Horizontal Acquisition: horizontal sync pulse coming out of the HIP
HFB	Horizontal Flyback Pulse: horizontal sync pulse from large signal deflection
HP	Headphone
Hue	Color phase control for NTSC (not the same as 'Tint')
I	Monochrome TV system. Sound carrier distance is 6.0 MHz
I2C	Integrated IC bus
IF	Intermediate Frequency
IIC	Integrated IC bus
Interlaced	Scan mode where two fields are used to form one frame. Each field contains half the number of the total amount of lines. The fields are written in 'pairs', causing line flicker.
ITV	Institutional TV
LATAM	Latin America
LED	Light Emitting Diode
L/L'	Monochrome TV system. Sound carrier distance is 6.5 MHz. L' is Band I, L is all bands except for Band I
LNA	Low Noise Amplifier
LS	Large Screen
LS	Loudspeaker
LSP	

	Large signal panel
M/N	Monochrome TV system. Sound carrier distance is 4.5 MHz
MSP	Multistandard Sound Processor: ITT sound decoder
MUTE	Mute-Line
NC	Not Connected
NICAM	Near Instantaneous Compounded Audio Multiplexing. This is a digital sound system, mainly used in Europe.
NTSC	National Television Standard Committee. Color system mainly used in North America and Japan. Color carrier NTSC M/N = 3.579545 MHz, NTSC 4.43 = 4.433619 MHz (this is a VCR norm, it is not transmitted off-air)
NVM	Non Volatile Memory: IC containing TV related data e.g. alignments
OB	Option Byte
OC	Open Circuit
OSD	On Screen Display
PAL	Phase Alternating Line. Color system mainly used in West Europe (color carrier = 4.433619 MHz) and South America (color carrier PAL M = 3.575612 MHz and PAL N = 3.582056 MHz)
PCB	Printed Circuit board
PIP	Picture In Picture
PLL	Phase Locked Loop. Used for e.g. FST tuning systems. The customer can give directly the desired frequency
POR	Power-On Reset
Progressive Scan	Scan mode where all scan lines are displayed in one frame at the same time, creating a double vertical resolution.
PTP	Picture Tube Panel (or CRT-panel)
RAM	Random Access Memory
RC	Remote Control handset
RC5	Remote Control system 5, signal from the remote control receiver
RGB	Red Green Blue

ROM	Read Only Memory
SAM	Service Alignment Mode
SAP	Second Audio Program
SC	Sandcastle: pulse derived from sync signals
S/C	Short Circuit
SCAVEM	Scan Velocity Modulation
SCL	Serial Clock
SDA	Serial Data
SDM	Service Default Mode
SECAM	SEquence Couleur Avec Memoire. Color system mainly used in France and East Europe. Color carriers = 4.406250 MHz and 4.250000 MHz
SIF	Sound Intermediate Frequency
SS	Small Screen
STBY	Standby
SVHS	Super Video Home System
SW	Software
THD	Total Harmonic Distortion
TXT	Teletext
uP	Microprocessor
UOC	Ultimate One Chip
VA	Vertical Acquisition
VBAT	Main supply voltage for the deflection stage (mostly 141 V)
V-chip	Violence Chip
VCR	Video Cassette Recorder
WYSIWYR	What You See Is What You Record: record selection that follows main picture and sound
XTAL	Quartz crystal
YC	Luminance (Y) and Chrominance (C) signal

IC Data Sheets

In this paragraph, the internal block diagrams and pinning are given of ICs that are drawn as a 'black box' in the electrical diagrams (with the exception of 'memory' and 'logic' ICs).

This is not applicable for this manual (all ICs are drawn with internal block diagrams)